T-52-33-03

M8744H
RUPI™-44: REMOTE UNIVERSAL PERIPHERAL INTERFACE

Military

- **M8744H–8044 with User Programmable/Erasable EPROM**
- **8-Bit CPU Plus Independent HDLC/SDLC Protocol Controller**
- **Serial Interface Unit (SIU)**
  - **—High-Performance, High-Level HDLC/SDLC Serial Communications Controller**
  - **—2.4 Mbps in Clocked Mode**
  - **—375 Kbps in Self Clocked Mode Using On-Chip Phase Lock Loop**
  - **—SDLC Loop Mode**
- **Fully Compatible with 8051 CPU**
- **Boolean Processor**
- **4K x 8 EPROM, 192 x 8 RAM**
- **External Memory Expandable to 128K Bytes**
- **32 I/O Lines, Configurable as a Local Bus**
- **Two 16-Bit Timer/Event Counters**
- **Military Temperature Range: −55°C to +125°C (T_C)**

The RUPI-44 is a Remote Universal Peripheral Interface designed to serve as a programmable remote peripheral or peripheral sub-system controller. It contains its own CPU, program memory, data memory, parallel I/O, timers/counters, and an intelligent serial interface that can serve as a primary or secondary station.

The CPU and all peripheral functions except for the data memory and the serial port are based on the 8051 and maintain complete compatibility with it. The data memory is larger (192 x 8) to allow convenient serial data buffering. The serial port implements a subset of HDLC/SDLC in the hardware. The Serial Interface Unit (SIU) operating concurrently with the CPU, offers a high level of intelligence and performance for HDLC/SDLC based communication.

The RUPI-44 devices are fabricated with Intel's reliable +5 volt, silicon-gate HMOS* technology and packaged in a 40-pin DIP.

*HMOS is a patented process of Intel Corporation.

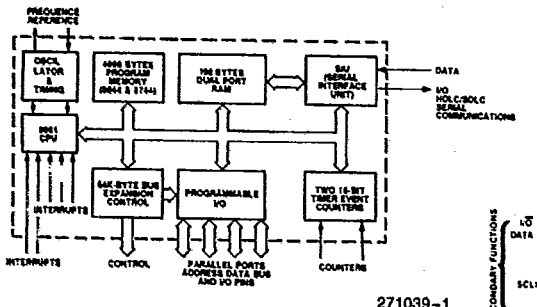

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Figure 1. Block Diagram

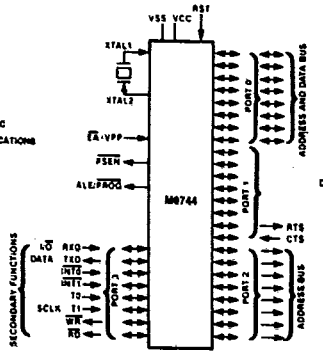

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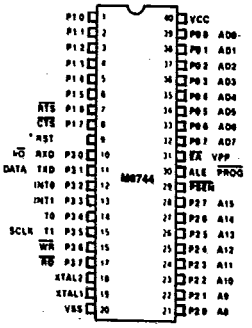
Figure 2. Logic Symbol



271039-3

Figure 3. Pin Configuration

December 1989
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M8744H Pin Description

V_{SS}
Circuit Ground Potential.

V_{CC}
+5V power supply during operation and program verification.

PORT 0
Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source six LS TTL loads.

PORT 1
Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.

In non-loop mode two of the I/O lines serve alternate functions:

— $\overline{RTS}$ (P1.6). Request-to-Send output. A low indicates that the RUPI-44 is ready to transmit.
— $\overline{CTS}$ (P1.7) Clear-to-Send input. A low indicates that a receiving station is ready to receive.

PORT 2
Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

PORT 3
Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads.

In addition to I/O, some of the pins also serve alternate functions as follows:

— $I/\overline{O}$ RxD (P3.0). In point-to-point or multipoint configurations, this pin controls the direction of pin P3.1. Serves as Receive Data input in loop and diagnostic modes.
— DATA TxD (P3.1) In point-to-point or multipoint configurations, this pin functions as data input/output. In loop mode, it serves as transmit pin. A '0' written to this pin enables diagnostic mode.
— $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.
— $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.
— TO (P3.4). Input to counter 0.
— SCLK T1 (P3.5). In addition to I/O, this pin provides input to counter 1 or serves as SCLK (serial clock) input.
— $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.
— $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST
A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pull-down resistor ($\approx$ 8.2 KΩ) from RST to V_{SS} permits power-on reset when a capacitor ($\approx$ 10 μF) is also connected from this pin to V_{CC}.

ALE/$\overline{PROG}$
Provides Address Latch Enable output used for latching the address into external memory during normal opertion. It is activated every six oscillator periods except during an external data memory access. It also receives the program pulse input for programming the M8744H.

$\overline{PSEN}$
The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

$\overline{EA}/V_{PP}$
When held at a TTL high level, the M8744H executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the RUPI-44 fetches all instructions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage on the M8744H.

XTAL 1
Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2.

XTAL 2
Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

FUNCTIONAL DESCRIPTION

General

The RUPI-44 integrates the powerful M8751 microcontroller with an intelligent Serial Interface Unit to provide a single-chip solution which will efficiently implement a distributed processing or distributed control system. The microcontroller is a self-sufficient unit containing ROM, RAM, ALU, and its own peripherals. The RUPI's architecture and instruction set are identical to the M8751's. The RUPI replaces the M8751's serial interface with an intelligent SDLC/HDLC Serial Interface Unit (SIU). 64 more bytes of RAM have been added to the M8751 RAM array. The SIU can communicate at bit rates up to 2.4 Mbps, clocked, or up to 375 Kbps, self clocked, using the on-chip digital phase locked loop. The SIU works concurrently with the Microcontroller so that there is no throughput loss in either unit. Since the SIU possesses its own intelligence, the CPU is offloaded from many of the communications tasks, thus dedicating more of its computing power to controlling local peripherals or some external process.

The Microcontroller

The microcontroller is stand-alone high-performance single-chip computer intended for use in sophisticated real-time application such as instrumentation, industrial control, and intelligent computer peripherals.

The major features of the microcontroller are:

- 8-bit CPU
- on-chip oscillator
- 4K bytes of EPROM
- 192 bytes of RAM
- 32 I/O lines
- 64K address space for external Data Memory
- 64K address space for external Program Memory
- two fully programmable 16-bit timer/counters
- a five-source interrupt structure with two priority levels
- bit addressability for Boolean processing
- 1 μs instruction cycle time for 60% of the instructions, 2 μs instruction cycle time for 40% of the instructions
- 4 μs cycle time for 8 by 8 bit unsigned Multiply/Divide

Parallel I/O

The M8744H has 32 general-purpose I/O lines which are arranged into four groups of eight lines. Each group is called a port. Hence there are four ports; Port 0, Port 1, Port 2, and Port 3. Up to five lines from Port 3 are dedicated to supporting the serial channel when the SIU is invoked. Due to the nature of the serial port, two of Port 3's I/O lines (P3.0 and P3.1) do not have latched outputs. This is true whether or not the serial channel is used.

Port 0 and Port 2 also have an alternate dedicated function. When placed in the external access mode, Port 0 and Port 2 become the means by which the RUPI communicates with external program memory. Port 0 and Port 2 are also the means by which the RUPI communicates with external data memory. Peripherals can be memory mapped into the address space and controlled by the RUPI.

Timer/Counters

The RUPI-44 contains two 16-bit counters which can be used for measuring time intervals, measuring pulse widths, counting events, generating precise periodic interrupt requests, and clocking the serial communications. Internally the Timers are clocked at 1/12 of the crystal frequency, which is the instruction cycle time. Externally the counters can run up to 500 KHz.

Interrupt System

External events and the real-time driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two priority level, nested interrupt system is provided. Interrupt response latency ranges from 3 μs to 6 μs when using a 10 MHz clock.

All five interrupt sources can be mapped into one of the two priority levels. Each interrupt source can be enabled or disabled individually or the entire interrupt system can be enabled or disabled. The five interrupt sources are: Serial interface Unit, Timer 1, Timer 2, and two external interrupts. The external interrupts can be either level or edge triggered.

Serial Interface Unit (SIU)

The Serial Interface Unit is used for HDLC/SDLC communications. It handles Zero Bit Insertion/Deletion, Flags, automatic address recognition, and a 16-bit cyclic redundancy check. In addition it implements in hardware a subset of the SDLC protocol such that it responds to many SDLC frames without CPU intervention. In certain applications it is advantageous to have the CPU control the reception or transmission of every single frame. For this reason the RUPI-44 has two modes of operation: "AUTO"

and "NON-AUTO". It is in the AUTO mode that the SIU responds to SDLC frames without CPU intervention; whereas, in the NON-AUTO mode the reception or transmission of every single frame will be under CPU control.

There are three control registers and eight parameter registers that are used to operate the serial interface. These registers are shown in Figure 4 and Figure 5. The control registers set the modes of operation and provide status information. The eight parameter registers buffer the station address, receive and transmit control bytes, and point to the on-chip transmit and receive buffers.

Data to be received or transmitted by the SIU must be buffered anywhere within the 192 bytes of on-chip RAM. Transmit and receive buffers are not allowed to "wrap around" in RAM; a "buffer end" is generated after address 191 is reached.

NON-AUTO Mode

In the NON-AUTO mode all communications are under control of the CPU. It is the CPU's task to encode and decode control fields, manage acknowledgements, and adhere to the requirements of the HDLC/SDLC protocols. The RUPI can be used as a primary or a secondary station in this mode.

To receive a frame in the NON-AUTO mode, the CPU must load the Receiver Buffer Start register, the Receive Buffer Length register, clear the Receive Buffer Protect bit, and set the Receiver Buffer Empty bit. If a valid opening flag is received and the address field matches the byte in the Station Address register or the address field contains a broadcast address, the RUPI loads the control field in the receive control byte register, and loads the I field in the receive buffer. If there is no CRC error, the SIU interrupts the CPU, indicating a frame has just been received. If there is a CRC error, the frame is ignored by the SIU and no interrupt occurs. The Receive Field Length register provides the number of bytes that were received in the information field.

To transmit a frame, the CPU must load the transmit information buffer, the Transmit Buffer Start register, the Transmit Buffer Length register, the Transmit Control Byte, and set the TBF and RTS bits. The SIU, unsolicited by an HDLC/SDLC frame, will transmit the entire information frame, and interrupt the CPU, indicating the completion of transmission. For supervisory frames or unnumbered frames, the transmit buffer length would be 0.

AUTO Mode

In the AUTO mode the SIU implements in hardware a subset of the SDLC protocol such that it responds to many SDLC frames without CPU intervention. All AUTO mode responses to the primary station will conform to IBM's SDLC definition. The advantages of the AUTO mode are that less software is required to implement a secondary station, and the hardware generated response to polls is much faster than doing it in software. However, the AUTO mode cannot be used as a primary station.

To transmit in the AUTO mode the CPU must load the Transmit Information Buffer, Transmit Buffer Start register, Transmit Buffer Length register, and set the Transmit Buffer Full bit. The SIU automatically responds to a poll by transmitting an information frame with the P/F bit in the control field set. When the SIU receives a positive acknowledgement from the primary station, it automatically increments the Ns field in the NSNR register and interrupts the CPU. A negative acknowledgement would cause the RUPI to re-transmit the frame.

To receive in the AUTO mode, the CPU loads the Receive Buffer Start register, the Receive Buffer Length register, clears the Receive Buffer Protect bit, and sets the Receive Buffer Empty bit. If the RUPI is polled in this state, and the TBF bit indicates that the Transmit Buffer is empty, an automatic RR response will be generated. When a valid information frame is received the SIU will automatically increment Nr in the NSNR register and interrupt the CPU.

While in the AUTO mode the SIU can recognize and respond to the following commands without CPU intervention: I (information), RR (Receive Ready), RNR (Receive Not Ready), REJ (Reject), and UP (Unnumbered Poll). The SIU can generate the following responses without CPU intervention: I (Information), RR (Receive Ready), and RNR (Receive Not Ready).

When the Receive Buffer Empty bit (RBE) indicates that the Receive Buffer is empty, the receiver is enabled, and when the RBE bit indicates that the Receive Buffer is full, the receiver is disabled. Assuming that the Receive Buffer is empty, the RUPI will respond to a poll with an I frame if the Transmit Buffer is full. If the Transmit Buffer is empty, the RUPI will respond to a poll with a RR command if the Receive Buffer Protect bit (RPB) is cleared, or an RNR command if RPB is set.

Frame Format Options

In addition to the standard SDLC frame format, the RUPI will support the frames displayed in Figure 6. The standard SDLC frame is shown at the top of this figure. For the remaining frames the information field will incorporate the control of address bytes and the frame check sequences; therefore these fields will

REGISTER NAMES	SYMBOLIC ADDRESS	BIT ADDRESS	BYTE ADDRESS
B REGISTER	B	247 through 240	240 (F0H)
ACCUMULATOR	ACC	231 through 224	224 (E0H)
*THREE BYTE FIFO	FIFO		223 (DFH)
	FIFO		222 (DEH)
	FIFO		221 (DDH)
TRANSMIT BUFFER START	TBS		220 (DCH)
TRANSMIT BUFFER LENGTH	TBL		219 (DBH)
TRANSMIT CONTROL BYTE	TCB		218 (DAH)
*SIU CONTROLLER STATE COUNTER	SIUST		217 (D9H)
SEND COUNT RECEIVE COUNT	NSNR	233 through 216	216 (D8H)
PROGRAM STATUS WORD	PSW	215 through 208	208 (D0H)
*DMA COUNT	DMA CNT		207 (CFH)
STATION ADDRESS	STAD		206 (CEH)
RECEIVE FIELD LENGTH	RFL		205 (CDH)
RECEIVE BUFFER START	RBS		204 (CCH)
RECEIVE BUFFER LENGTH	RBL		203 (CBH)
RECEIVE CONTROL BYTE	RCB		202 (CAH)
SERIAL MODE	SMD		201 (C9H)
STATUS REGISTER	STS	207 through 200	200 (C8H)
INTERRUPT PRIORITY CONTROL	IP	191 through 184	184 (B8H)
PORT 3	P3	183 through 176	176 (B0H)
INTERRUPT ENABLE CONTROL	IE	175 through 168	168 (A8H)
PORT 2	P2	167 through 160	160 (A0H)
PORT 1	P1	151 through 144	144 (90H)
TIMER HIGH 1	TH1		141 (8DH)
TIMER HIGH 0	TH0		140 (8CH)
TIMER LOW 1	TL1		139 (8BH)
TIMER LOW 0	TL0		138 (8AH)
TIMER MODE	TMOD		137 (89H)
TIMER CONTROL	TCON	143 through 136	136 (88H)
DATA POINTER HIGH	DPH		131 (83H)
DATA POINTER LOW	DPL		130 (82H)
STACK POINTER	SP		129 (81H)
PORT 0	P0	135 through 128	128 (80H)

SFR'S CONTAINING DIRECT ADDRESSABLE BITS

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*ICE Support Hardware registers. Under normal operating conditions there is no need for the CPU to access these registers.

Figure 4. Mapping of Special Function Registers

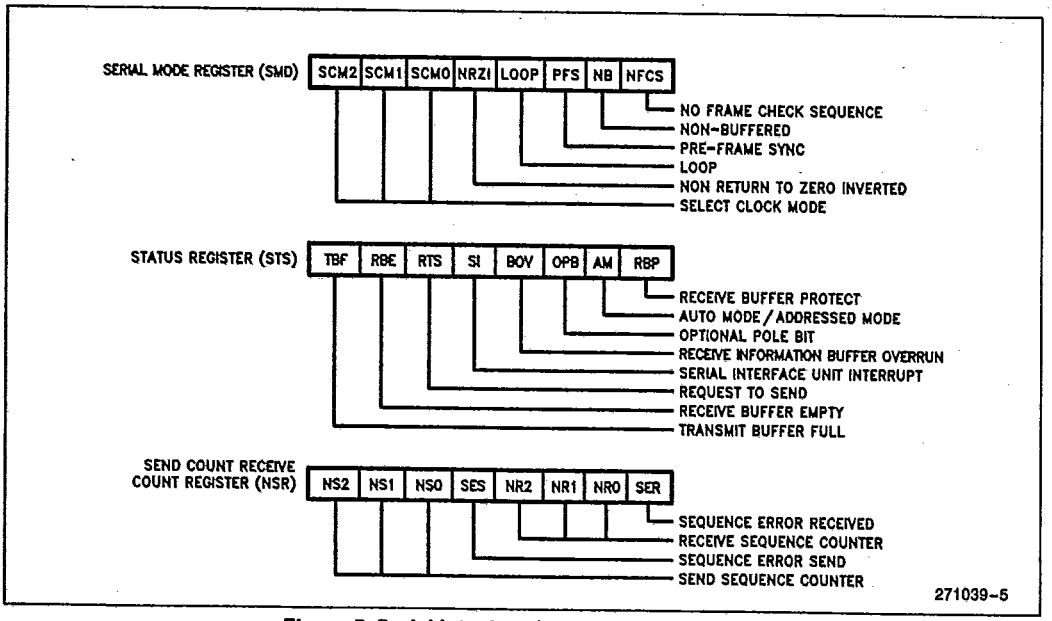


Figure 5. Serial Interface Unit Control Registers

be stored in the Transmit and Receive Buffers. For example, in the non-buffered mode the third byte is treated as the beginning of the information field. In the non-addressed mode, the information field begins after the opening flag. The mode bits to set the frame format options are found in the Serial Mode register and the Status register.

HDLC (Extended Addressing)

To realize an extended control field or an extended address field using the HDLC protocol, the NON-AUTO mode must be used. For an extended control field, the RUPI is programmed to be in the non-buffered mode. The extended control field will be the first and second bytes in the Receive and Transmit Buffers. For extended addressing the RUPI is placed in the non-addressed mode. In this mode the CPU must implement the address recognition for received frames. The addressing field will be the initial bytes in the Transmit and Receive Buffers followed by the control field.

The RUPI can transmit and receive only frames which are multiples of 8 bits. For frames received with other than 8-bit multiples, a CRC error will cause the SIU to reject the frame.

SDLC Loop Networks

The RUPI can be used in a SDLC loop as a secondary or primary station. When the RUPI is placed in the Loop mode it receives the data on pin 10 and transmits the data one bit time delayed on pin 11. It can also recognize the Go Ahead signal and change it into a flag when it is ready to transmit. As a secondary station the RUPI can be used in the AUTO or NON-AUTO modes. As a primary station the NON-AUTO mode is used; however, additional hardware is required for generating the Go Ahead bit pattern. In the Loop mode the maximum data rate is 1 Mbps clocked or 375 Kbps self-clocked.

FRAME OPTION	NFCS	NB	AM(1)	FRAME FORMAT
Standard SDLC NON-AUTO Mode	0	0	0	F A C I FCS F
Standard SDLC AUTO Mode	0	0	1	F A C I FCS F
Non-Buffered Mode NON-AUTO Mode	0	1	1	F A I FCS F
Non-Addressed Mode NON-AUTO Mode	0	1	0	F I FCS F
No FCS Field NON-AUTO Mode	1	0	0	F A C I F
No FCS Field AUTO Mode	1	0	1	F A C I F
No FCS Field Non-Buffered Mode NON-AUTO Mode	1	1	1	F A I F
No FCS Field Non-Addressed Mode NON-AUTO Mode	1	1	0	F I F

Mode Bits:
AM — "AUTO" Mode/Addressed Mode
NB — Non-Buffered Mode
NFCS — No FCS Field Mode

Key to Abbreviations:
F = FLAG (01111110)
A = Address Field
C = Control Field
I = Information Field
FCS = Frame Check Sequence

NOTE:
1. The AM bit function is controlled by the NB bit. When NB = 0, AM becomes AUTO mode select, when NB = 1, AM becomes Address mode select.

Figure 6. Frame Format Options

SDLC Multidrop Networks

The RUPI can be used in a SDLC non-loop configuration as a secondary or primary station. When the RUPI is placed in the non-loop mode, data is received and transmitted on pin 11, and pin 10 drives a tri-state buffer. In non-loop mode, modern interface pins, $\overline{RTS}$ and $\overline{CTS}$, become available.

Data Clocking Options

The RUPI's serial port can operate in an externally clocked or self clocked system. A clocked system provides to the RUPI a clock synchronized to the data. A self-clocked system uses the RUPI's on-chip Digital Phase Locked Loop (DPLL) to recover the clock from the data, and clock this data into the Serial Receive Shift Register.

Clocked Mode

In this mode, a clock synchronized with the data is externally fed into the RUPI. This clock may be generated from an External Phase Locked Loop, or possibly supplied along with the data. The RUPI can transmit and receive data in this mode at rates up to 2.4 Mbps.

Self Clocked Mode

This mode allows data transfer without a common system data clock. An on-chip Digital Phase Locked Loop is employed to recover the data clock which is inherent in the data stream. The DPLL will converge to the nominal bit center within eight bit transitions, worst case. The DPLL requires a reference clock of either 16 times (16×) or 32 times (32×) the data rate. This reference clock may be externally applied or internally generated. When internally generated either the RUPI's internal logic clock (crystal frequency divided by two) or the timer 1 overflow is used as the reference clock. Using the internal timer 1 clock the data rates can vary from 244 Kbps to 62.5 Kbps. Using the internal logic clock at a 16 × sampling rate, receive data can either be 187.5 Kbps, or 375 Kbps. When the reference clock for the DPLL is externally applied the data rates can vary from 0 to 375 Kbps at a 16 × sampling rate.

To aid in a Phase Locked Loop capture, the RUPI has a NRZI (Non Return to Zero Inverted) data encoding and decoding option. Additionally the RUPI has a pre-frame sync option that transmits two bytes of alternating 1's and 0's to ensure that the receive station DPLL will be synchronized with the data by the time it receives the opening flag.

Control and Status Registers

There are three SIU Control and Status Registers:
Serial Mode Register (SMD)
Status/Command Register (STS)
Send/Receive Count Register (NSNR)

The SMD, STS, and NSNR registers are all cleared by system reset. This assures that the SIU will power up in an idle state (neither receiving nor transmitting).

These registers and their bit assignments are described below.

SMD: Serial Mode Register (byte-addressable)

Bit: 7	6	5	4	3	2	1	0
SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

The Serial Mode Register (Address C9H) selects the operational modes of the SIU. The 8044 CPU can both read and write SMD. The SIU can read SMD but cannot write to it. To prevent conflict between CPU and SIU access to SMD, the CPU should write SMD only when the Request To Send (RTS) and Receive Buffer Empty (RBE) bits (in the STS register) are both false (0). Normally, SMD is accessed only during initialization.

The individual bits of the Serial Mode Register are as follows:

Bit #	Name	Description
SMD.0	NFCS	No FCS field in the SDLC frame.
SMD.1	NB	Non-Buffered mode. No control field in the SDLC frame.
SMD.2	PFS	Pre-Frame Sync mode. In this mode, the 8044 transmits two bytes before the first flag of a frame, for DPLL synchronization. If NRZI is enabled, 00H is sent; otherwise, 55H is sent. In either case, 16 preframe transitions are guaranteed.
SMD.3	LOOP	Loop configuration.
SMD.4	NRZI	NRZI coding option. If bit = 1, NRZI coding is used. If bit = 0, then it is straight binary (NRZ).
SMD.5	SCM0	Select Clock Mode—Bit 0
SMD.6	SCM1	Select Clock Mode—Bit 1
SMD.7	SCM2	Select Clock Mode—Bit 2

The SCM bits decode as follows:

SCM 2	SCM 1	SCM 0	Clock Mode	Data Rate (Bits/Sec)*
0	0	0	Externally Clocked	0–2.4M**
0	0	1	Reserved	
0	1	0	Self Clocked, Timer Overflow	244–62.5K
0	1	1	Reserved	
1	0	0	Self Clocked, External 16×	0–375K
1	0	1	Self Clocked, External 32×	0–187.5K
1	1	0	Self Clocked, Internal Fixed	375K
1	1	1	Self Clocked, Internal Fixed	187.5K

NOTES:
*Based on a 12 MHz crystal frequency
**0–1 Mbps in loop configuration

STS: Status/Command Register (bit-addressable)

Bit: 7	6	5	4	3	2	1	0
TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

The Status/Command Register (Address C8H) provides operational control of the SIU by the 8044 CPU, and enables the SIU to post status information for the CPU's Access. The SIU can read STS, and can alter certain bits, as indicated below. The CPU can both read and write STS asynchronously. However, 2-cycle instructions that access STS during both cycles ('JBC/B, REL' and 'MOV/B, C.') should not be used since the SIU may write to STS between the two CPU accesses.

The individual bits of the Status/Command Register are as follows:

Bit #	Name	Description
STS.0	RBP	Receive Buffer Protect. Inhibits writing of data into the receive buffer. In AUTO mode, RBP forces an RNR response instead of an RR.
STS.1	AM	AUTO Mode/Addressed Mode. Selects AUTO mode where AUTO mode is allowed. If NB is true, (= 1), the AM bit selects the addressed mode. AM may be cleared by the SIU.
STS.2	OPB	Optional Poll Bit. Determines whether the SIU will generate an AUTO response to an optional poll (UP with P = 0). OPM may be set or cleared by the SIU.
STS.3	BOV	Receive Buffer Overrun. BOV may be set or cleared by the SIU.
STS.4	SI	SIU Interrupt. This is one of the five interrupt sources to the CPU. The vector location = 23H. SI may be set by the SIU. It should be cleared by the CPU before returning from an interrupt routine.
STS.5	RTS	Request To Send. Indicates that the 8044 is ready to transmit or is transmitting. RTS may be read or written by the CPU. RTS may be read by the SIU, and in AUTO mode may be written by the SIU.
STS.6	RBE	Receive Buffer Empty. RBE can be thought of as Receive Enable. RBE is set to one by the CPU when it is ready to receive a frame, or has just read the buffer, and to zero by the SIU when a frame has been received.
STS.7	TBF	Transmit Buffer Full. Written by the CPU to indicate that it has filled the transmit buffer. TBF may be cleared by the SIU.

NSNR: Send/Receive Count Register (bit-addressable)

Bit: 7	6	5	4	3	2	1	0
NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

The Send/Receive Count Register (Address D8H) contains the transmit and receive sequence numbers, plus tally error indications. The SIU can both read and write NSNR. The 8044 CPU can both read and write NSNR asynchronously. However, 2-cycle instructions that access NSNR during both cycles ('JBC/B, REL,' and 'MOV /B,C') should not be used, since the SIU may write to NSMR between the two 8044 CPU accesses.

The individual bits of the Send/Receive Count Register are as follows:

Bit #	Name	Description
NSNR.0	SER	Receive Sequence Error: NS (P) ≠ NR (S)
NSNR.1	NR0	Receive Sequence Counter—Bit 0
NSNR.2	NR1	Receive Sequence Counter—Bit 1
NSNR.3	NR2	Receive Sequence Counter—Bit 2
NSNR.4	SES	Send Sequence Error: NR (P) ≠ NS (S) and NR (P) ≠ NS (S) + 1
NSNR.5	NS0	Send Sequence Counter—Bit 0
NSNR.6	NS1	Send Sequence Counter—Bit 1
NSNR.7	NS2	Send Sequence Counter—Bit 2

Parameter Registers

There are eight parameter registers that are used in connection with SIU operation. All eight registers may be read or written by the 8044 CPU. RFL and RCB are normally loaded by the SIU.

The eight parameter registers are as follows:

STAD: Station Address Register (byte-addressable)

The Station Address Register (Address CEH) contains the station address. To prevent access conflict, the CPU should access STAD only when the SIU is idle (RTS = 0 and RBE = 0). Normally, STAD is accessed only during initialization.

TBS: Transmit Buffer Start Address Register (byte-addressable)

The Transmit Buffer Start Address Register (Address DCH) points to the location in on-chip RAM for the beginning of the I-field of the frame to be transmitted. The CPU should access TBS only when the SIU is not transmitting a frame (whe TBF = 0).

TBL: Transmit Buffer Length Register (byte-addressable)

The Transmit Buffer Length Register (Address DBH) contains the length (in bytes) of the I-field to be transmitted. A blank I-field (TBL = 0) is valid. The CPU should access TBL only when the SIU is not transmitting a frame (when TBF = 0).

NOTE:
The transmit and receive buffers are not allowed to "wrap around" in the on-chip RAM. A "buffer end" is automatically generated if address 191 (BFH) is reached.

TCB: Transmit Control Byte Register (byte-addressable)

The Transmit Control Byte Register (Address DAH) contains the byte which is to be placed in the control field of the transmitted frame, during NON-AUTO mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame (when TBF = 0). The N_S and N_R counters are not used in the NON-AUTO mode.

RBS: Receive Buffer Start Address Register (byte-addressable)

The Receive Buffer Start Address Register (Address CCH) points to the location in on-chip RAM where the beginning of the I-field of the frame being received is to be stored. The CPU should write RBS only when the SIU is not receiving a frame (when RBE = 0).

RBL: Receive Buffer Length Register (byte-addressable)

The Receive Buffer Length Register (Address CBH) contains the length (in bytes) of the area in on-chip RAM allocated for the received I-field. RBL = 0 is valid. The CPU should write RBL only when RBE = 0.

RFL: Receive Field Length Registers (byte-addressable)

The Receive Field Length Register (Address CDH) contains the length (in bytes) of the received I-field that has just been loaded into on-chip RAM. RFL is loaded by the SIU. RFL = 0 is valid. RFL should be accessed by the CPU only when RBE = 0.

RCB: Receive Control Byte Register (byte-addressable)

The Received Control Byte Register (Address CAH) contains the control field of the frame that has just been received. RCB is loaded by the SIU. The CPU can only read RCB, and should only access RCB when RBE = 0.

ICE Support

The 8044 In-Circuit Emulator (ICE-44) allows the user to exercise the 8044 application system and monitor the execution of instructions in real time.

The emulator operates with Intel's Intellec™ development system. The development system interfaces with the user's 8044 system through an in-cable buffer box. The cable terminates in an 8044 pin-compatible plug, which fits into the 8044 socket in the user's system. With the emulator plug in place, the user can exercise his system in real time while collecting up to 255 instruction cycles of real-time data. In addition, he can single-step the program.

Static RAM is available (in the in-cable buffer box) to emulate the 8044 internal and external program memory and external data memory. The designer can display and alter the contents of the replacement memory in the buffer box, the internal data memory, and the internal 8044 registers, including the SFR's.

SIUST: SIU State Counter (byte-addressable)

The SIU State Counter (Address D9H) reflects the state of the internal logic which is under SIU control. Therefore, care must be taken not to write into this register. This register provides a useful means for debugging 8044 receiver problems.

M8744H EPROM CHARACTERISTICS

Erasure Characteristics

Erasure of the M8744H Program Memory begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wave-lengths in this range, constant exposure to these light sources over an extended period of time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause unintentional erasure. If an application subjects the M8744H to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Programming the EPROM

To be programmed, the M8744H must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0–P2.3 of Port 2, while the data byte is applied to Port 0. Pins P2.4–P2.6 and $\overline{\text{PSEN}}$ should be held low, and P2.7 and RST high. (These are all TTL levels except RST, which requires 2.5V for high.) $\overline{\text{EA}}$/VPP is held normally high, and is pulsed to +21V. While EA/VPP is at 21V, the ALE/$\overline{\text{PROG}}$ pin, which is normally being held high, is pulsed low for 50 ms. The EA/VPP is returned to high. Detailed timing specifications are provided in the EPROM Programming and Verification Characteristics section of this data sheet.

Program Memory Security

The program memory security feature is developed around a "security bit" in the M8744H EPROM array. Once this "hidden bit" is programmed, electrical access to the contents of the entire program memory array becomes impossible. Activation of this feature is accomplished by programming the M8744H as described in "Programming the EPROM" with the exception that P2.6 is held at a TTL high rather than a TTL low. In addition, Port 1 and P2.0–P2.3 may be in any state. Deactivating the security feature, which again allows programmability of the EPROM, is accomplished by exposing the EPROM to ultraviolet light. This exposure, as described in "Erasure Characteristics," erases the entire EPROM array. Therefore, attempted retrieval of "protected code" results in its destruction.

Program Verification

Program Memory may be read only when the "security feature" has not been activated. To read the Program Memory, the following procedure can be used. The unit must be running with a 4 to 6 MHz oscillator. The address of a Program Memory location to be read is applied to Port 1 and pins P2.0–P2.3 of Port 2. Pins P2.4–P2.6 and $\overline{\text{PSEN}}$ are held at TTL low, while the ALE/$\overline{\text{PROG}}$, RST, and $\overline{\text{EA}}$/VPP pins are held at TTL high. (These are all TTL levels except RST, which requires 2.5V for high.) Port 0 will be the data output lines. P2.7 can be used as a read strobe. While P2.7 is held high, the Port 0 pins float. When P2.7 is strobed low, the contents of the addressed location will appear at Port 0. External pull-ups (e.g., 10K) are required on Port 0 during program verification.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature
Under Bias .....−55°C to +125°C
Storage Temperature .....−65°C to +150°C
Maximum Voltage V_{PP} to V_{SS} 21.5V
Voltage on Any Pin with Respect to Ground (V_{SS})(except $\overline{EA}$) .....−0.5V to +7V
Power Dissipation 2W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{IL}	Input Low Voltage	−0.5		0.7	V	
V_{IH}	Input High Voltage (Except RST/V_{PD} and XTAL2)	2.2		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage to RST/V_{PD} for Reset, XTAL2	2.5			V	XTAL1 to V_{SS}
V_{OL}	Output Low Voltage Ports 1, 2, 3 (Note 1)			0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output Low Voltage Port 0, ALE, /$\overline{PSEN}$ (Note 1)			0.45	V	I_{OL} = 2.4 mA
V_{OH}	Output High Voltage Ports 1, 2, 3	2.4			V	I_{OH} = −80 μA
V_{OH1}	Output High Voltage Port 0, ALE, /$\overline{PSEN}$	2.4			V	I_{OH} = −400 μA
I_{IL}	Logical 0 Input Current Ports 1, 2, 3 (Note 2)			−500	μA	V_{in} = 0.45V
I_{IH1}	Input High Current to RST/V_{PD} for Reset			500	μA	V_{in} = V_{CC} −1.5V
I_{LI}	Input Leakage Current to Port 0			125	μA	0.45 < V_{in} < V_{CC}
I_{CC}	Power Supply Current			300	mA	
CIO	Capacitance of $\overline{I/O}$ Buffer			10	pF	Test Freq = 1 MHz
I_{IL2}	Logical 0 Input Current XTAL 2			−3.5	mA	XTAL1 = V_{SS} V_{IL} = 0.45V
V_{IL1}	Input Low Voltage to $\overline{EA}$/V_{PP}	0		0.7	V	
I_{IL1}	Logical 0 Input Current to $\overline{EA}$/V_{PP}			−15	mA	V_{in} = 0.45V
I_{IH}	Logical Input Current to $\overline{EA}$/V_{PP}			500	μA	

NOTES:
1. V_{OL} is degraded when the RUPI-44 rapidly discharges external capacitance. This A.C. noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the RUPI-44 as possible.
2. Except P1.6 (Pin 7), P3.0 (Pin 10) and P3.1 (Pin 11) = −700 μA max.

Datum	Emitting Ports	Time Interval	Degraded I/O Lines	V_{OL} (Peak) (Max)
Address	P2, P0	T3, T9	P1, P3	0.8V
Write Data	P0	T6	P1, P3, ALE	0.8V

A.C. CHARACTERISTICS (Over Specified Operating Conditions) C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF

PROGRAM MEMORY TIMING

Symbol	Parameter	Variable Clock 1/TCLCL = 6 MHz to 10 MHz		
		Min	Max	Units
TLHLL	ALE Pulse Width	2TCLCL-40		ns
TAVLL	Address Setup to ALE	TCLCL-40		ns
TLLAX(2)	Address Hold After ALE	4TCLCL-35		ns
TLLIV	ALE to Valid Instr In		4TCLCL-150	ns
TLLPL	ALE to $\overline{PSEN}$	TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	3TCLCL-60		ns
TPLIV	$\overline{PSEN}$ to Valid Instr In		3TCLCL-150	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns
TPXIZ(3)	Input Instr Float After $\overline{PSEN}$		TCLCL-20	ns
TPXAV(3)	Address Valid After $\overline{PSEN}$	TCLCL-8		ns
TAVIV	Address to Valid Instr In		5TCLCL-150	ns
TAZPL	Address Float to $\overline{PSEN}$	−25		ns

EXTERNAL DATA MEMORY TIMING

Symbol	Parameter	Variable Clock 1/TCLCL = 6 MHz to 10 MHz		
		Min	Max	Units
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL-100		ns
TLLAX(2)	Address Hold After ALE	TCLCL-35		
TRLDV	$\overline{RD}$ to Valid Data In		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL-70	ns
TLLDV	ALE to Valid Data In		8TCLCL-150	ns
TAVDV	Address to Valid Data In		9TCLCL-165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL-130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE HIGH	TCLCL-50	TCLCL+50	ns
TDVWX	Data Valid to $\overline{WR}$ Transition	TCLCL-70		ns
TQVWH	Data Setup Before $\overline{WR}$	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		25	ns

NOTES:
1. TLLAX for access to program memory is different from TLLAX for data memory.
2. Interfacing RUPI-44 devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

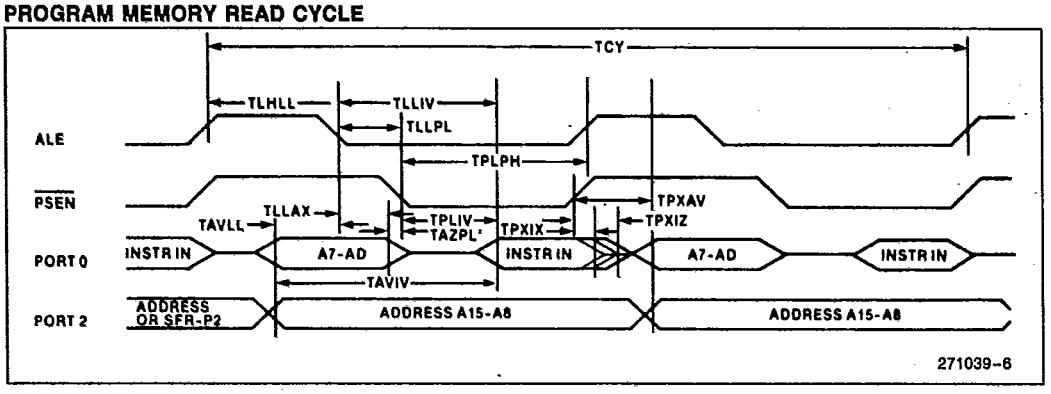
SERIAL INTERFACE TIMING

Symbol	Parameter	Min	Max	Units
t_{DCY}	Data Clock	420		ns
t_{DCL}	Data Clock Low	180		ns
t_{DCH}	Data Clock High	100		ns
t_{TD}	Transmit Data Delay		180	ns
t_{DSS}	Data Setup Time	40		ns
t_{DHS}	Data Hold Time	40		ns

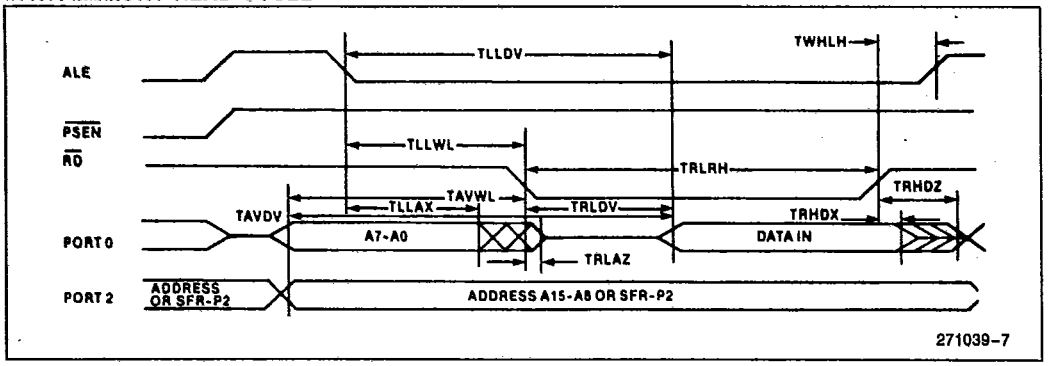
WAVEFORMS

MEMORY ACCESS

PROGRAM MEMORY READ CYCLE



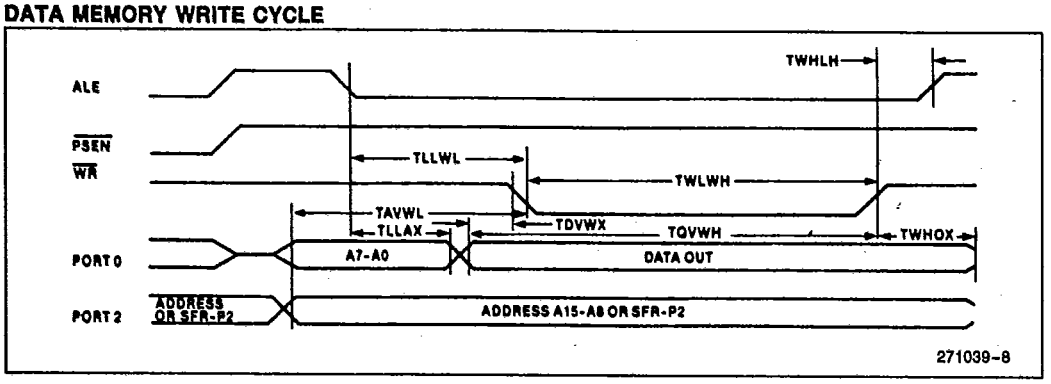
DATA MEMORY READ CYCLE



WAVEFORMS (Continued)

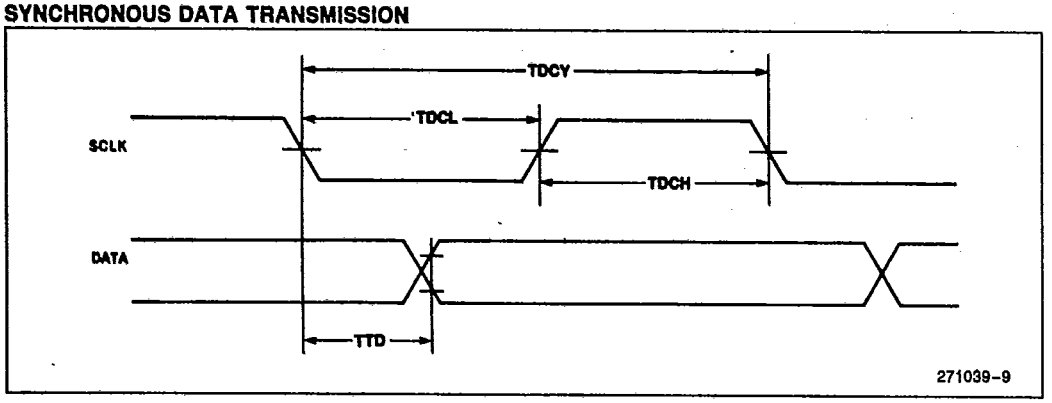
MEMORY ACCESS (Continued)

DATA MEMORY WRITE CYCLE

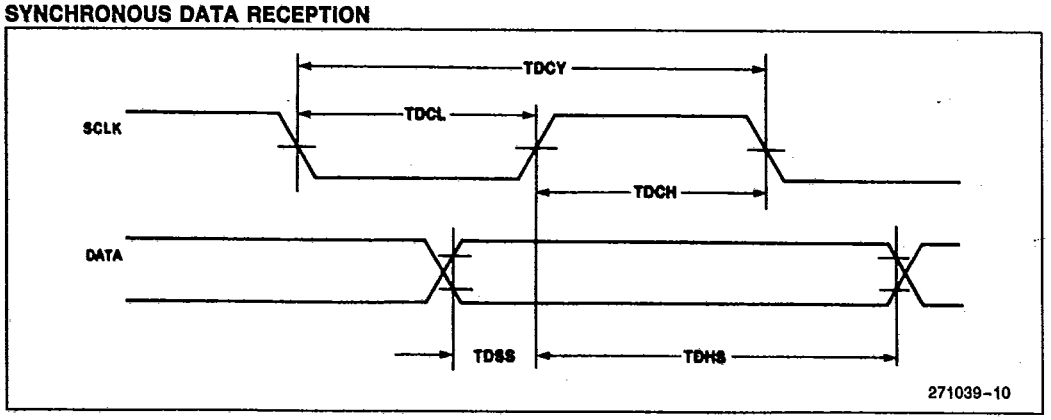


SERIAL I/O WAVEFORMS

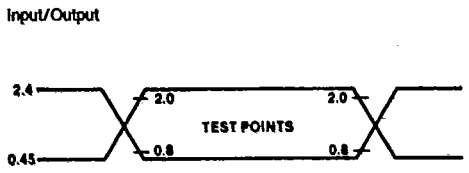
SYNCHRONOUS DATA TRANSMISSION



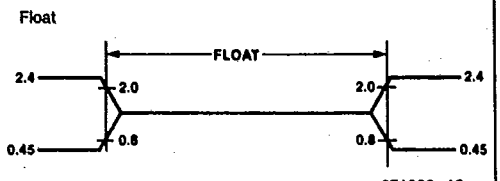
SYNCHRONOUS DATA RECEPTION



A.C. TESTING INPUT, OUTPUT, FLOAT WAVEFORMS



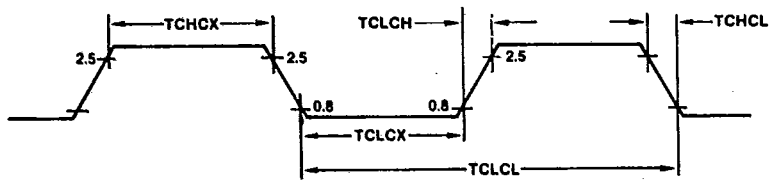
271039-11



271039-12

A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 μA at the voltage test levels.

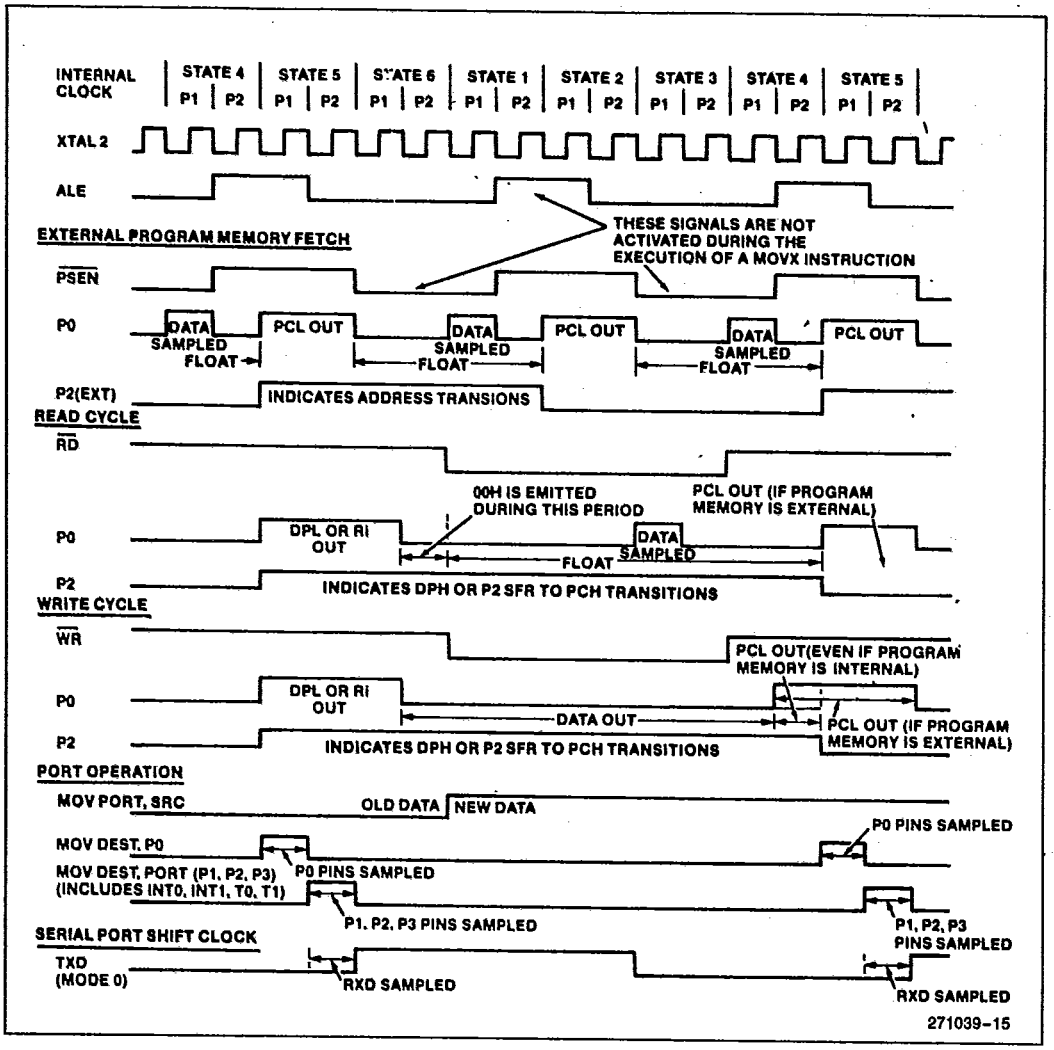
EXTERNAL CLOCK DRIVE XTAL2



271039-13

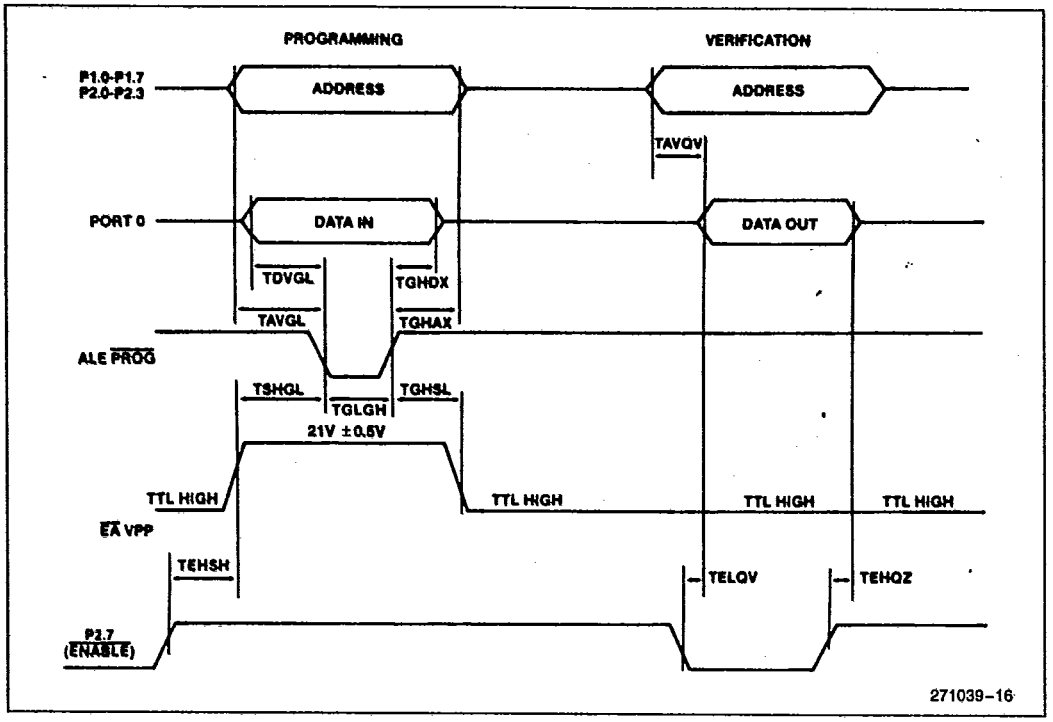
Symbol	Parameter	Variable Clock Freq = 6 MHz to 10 MHz		Unit
		Min	Max	
TCLCL	Oscillator Period	100	167	ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCLCL	Fall Time		20	ns

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 50 ns to 150 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

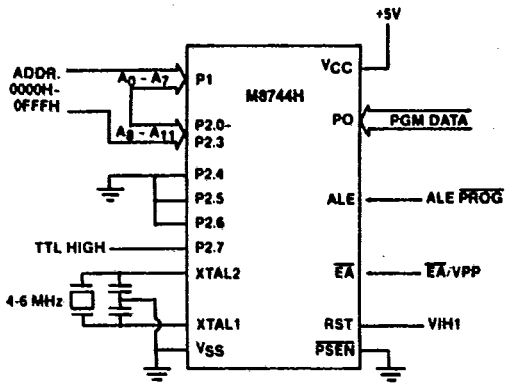
EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION WAVEFORMS



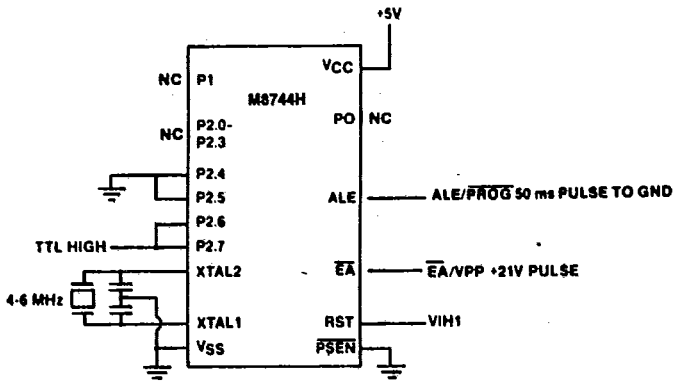
EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION CHARACTERISTICS T_A = 21°C to 27°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	20.5	21.5	V
I_{PP}	Programming Current		30	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	$\overline{ENABLE}$ High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	45	55	ms
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ to Data Valid		48TCLCL	
TEHQZ	Data Float after $\overline{ENABLE}$	0	48TCLCL	

PROGRAMMING CONFIGURATION



SECURITY BIT PROGRAMMING CONFIGURATION



PROGRAM VERIFICATION CONFIGURATION